AMENDMENTS

In the Specification

CA 2/15/06

Please add the following paragraph after line 8, page 6:

FIG. 10B is a cross-section of forming the CPU scheme under two layers of conductive ring.

Please amend the paragraph beginning on page 10, line 27 as follows:

FIG. 3A is a cross-section of another conductive ring underlying the conductive ring 26. Elements similar to those in FIG. 2A are omitted here. A second dielectric layer 36 underlying the first dielectric layer 24 is provided. A third conductive layer 38 is patterned as a ring and embedded in the second dielectric layer 36. A conductive plug 40 also is formed in the second dielectric layer 36 to electrically connect the conductive ring 26 to the ~~second~~ third conductive layer 38.

Please amend the paragraph beginning on page 11, line 6 as follows:

FIG. 3B is a cross-section of a conductive lattice underlying the conductive ring 26. Elements similar to those in FIG. 3A are omitted here. The third conductive layer 38 is modified to form a lattice, in which an array of dielectric islands 36a is provided and the dielectric islands 36a are spaced apart from each other by the third conductive layer 38. Alternately, the third conductive layer 38 is modified to form an array of independent plugs spaced apart from each other by the second dielectric layer 36.